EES271: Digital Circuits
Final Mock Exam

from James Dean and Google and The Peanuts

Name . . . . ID . . . . Section . . . .

Conditions: Closed Book, Calculator Allowed

Directions:

1. This exam has 22 pages (including this page).
2. Students are encouraged to dramatically sigh every time a K-map has more than 4 variables (good luck with that).
3. Write your name, or your preferred truth table alias.
4. Reading the problem is optional but highly recommended. Skipping it may leave you in a race condition.
5. Students may not escape through windows, air vents
6. If you latch onto the wrong solution, reset yourself and try again—sequential circuits forgive but don't forget.

Disclaimer

This mock examination has been created to help you prepare for your upcoming Digital Circuits exam. Please note the following:

- Parts or whole sections of this mock exam have been adapted and modified from Aj. Itthisek Nilkhamhang's course materials and exercises. All credits and acknowledgments go to Aj. Itthisek.
- An appendix containing *truth tables, transition tables, list of boolean algebraic laws* has been provided at the back of this mock exam. This appendix mirrors what will be available in your actual examination.
- Truth table templates have been included to save you time from drawing tables. Please note that these templates may or may not be provided in the actual exam - they are included here purely to help you focus on solving the problems rather than drawing tables.
- If you find any errors, inconsistencies, or have questions about the problems, please don't hesitate to contact me. Your feedback helps improve the quality of these practice materials.
- This mock exam aims to simulate the actual exam environment. The difficulty level and question style have been designed to match what you can expect in the final examination.

Best of luck with your preparation!

Truth Table Template

2-Variable Truth Table

(inputs go here) (output goes here)

0	**0**		
0	**1**		
1	**0**		
1	**1**		

3-Variable Truth Table

(inputs go here) (output goes here)

0	**0**	**0**		
0	**0**	**1**		
0	**1**	**0**		
0	**1**	**1**		
1	**0**	**0**		
1	**0**	**1**		
1	**1**	**0**		
1	**1**	**1**		

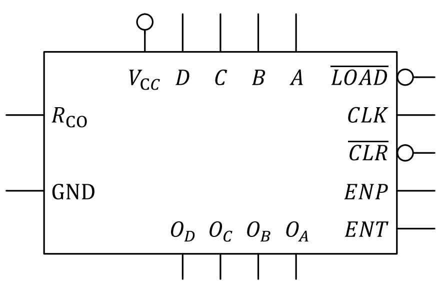
4-Variable Truth Table

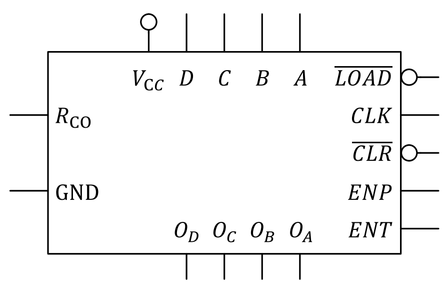
(inputs go here) (output goes here)

0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Problem 1

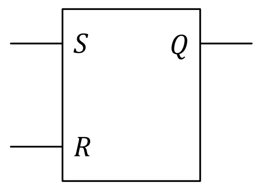
Design a truncated sequence counter that counts from 0 to 15 and then from 50 to 63. Once the count reaches 63, the counter should repeat the sequence from 0.

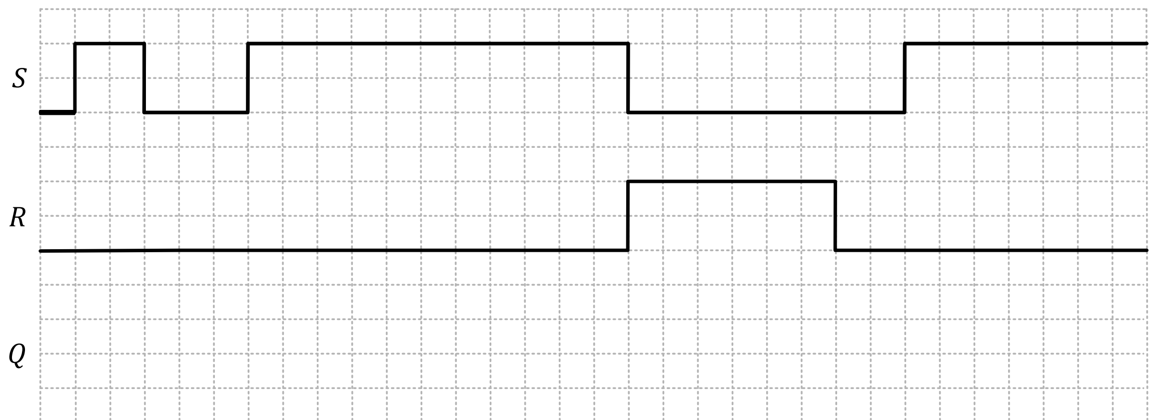




Problem 2

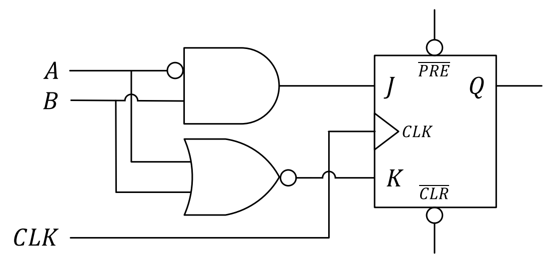
Determine and draw the output waveform Q if the signals shown below are applied to the inputs of an S-R latch. Assume that Q is initially LOW.

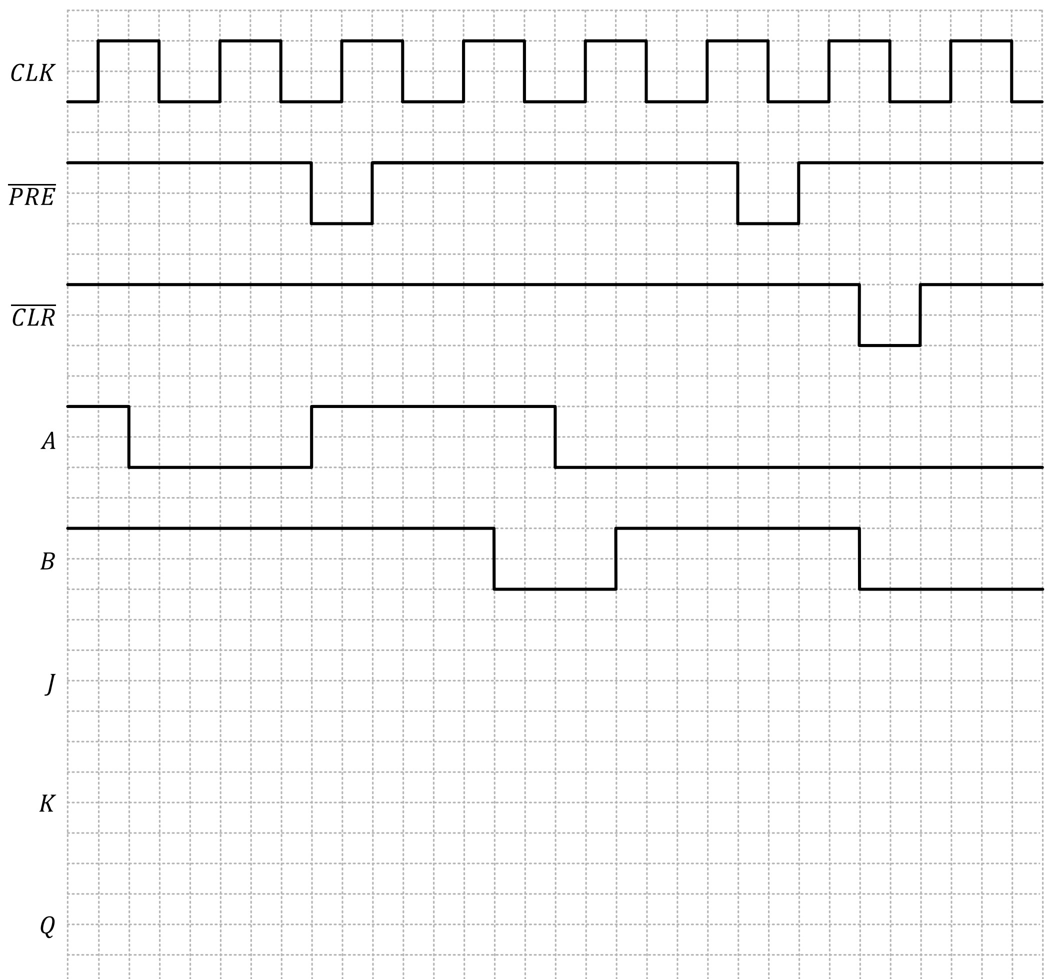




Problem 3

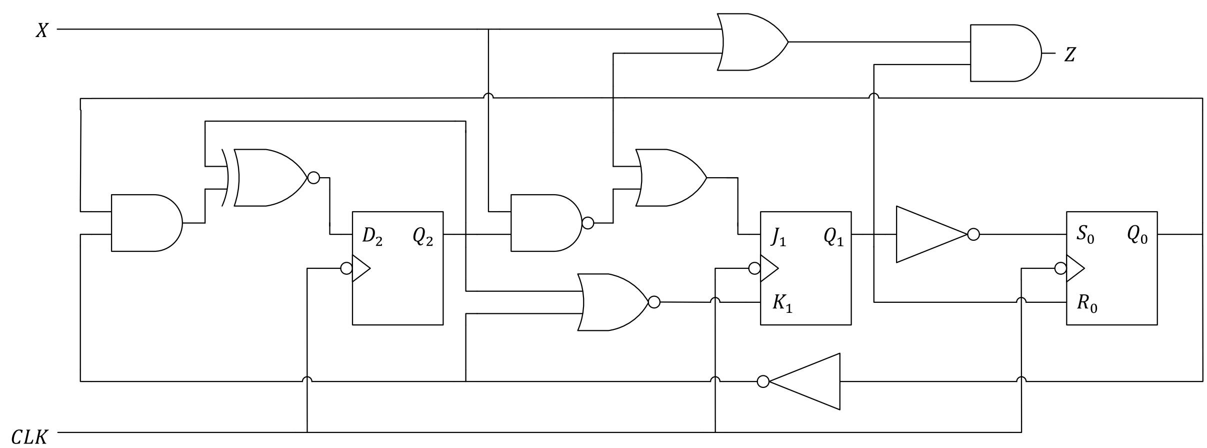
Determine and draw the specified waveforms (J, K, and Q) if the following signals are applied to the circuit shown below. Assume that Q is initially LOW.





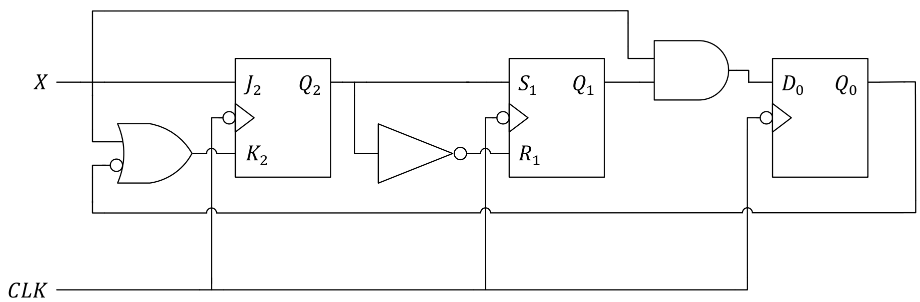
Problem 4

Consider the following sequential logic circuit. Let the input to the system be denoted as X, and the output of the system be denoted as Z. Use $Q_2Q_1Q_0$ and $Q_2^*Q_1^*Q_0^*$ to represent the current and next states. **Derive the state table and state diagram.**



Problem 5

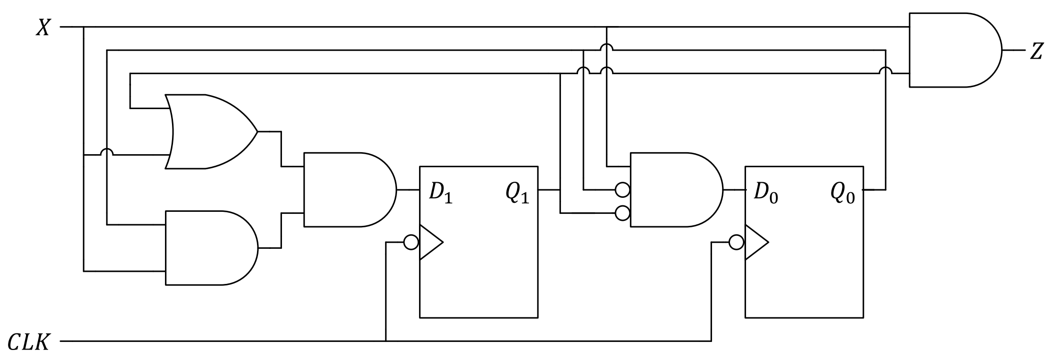
Consider the following sequential logic circuit. Let the input to the system be denoted as X. Use the codes $Q_2Q_1Q_0$ and $Q_2^*Q_1^*Q_0^*$ to represent the current and next states. There are no outputs from the system. **Derive the state table and state diagram.** Complete the **timing trace**



X	0	0	1	0	1	0	1	?	?
Q_2	0								
Q_1	0								
Q_0	0								

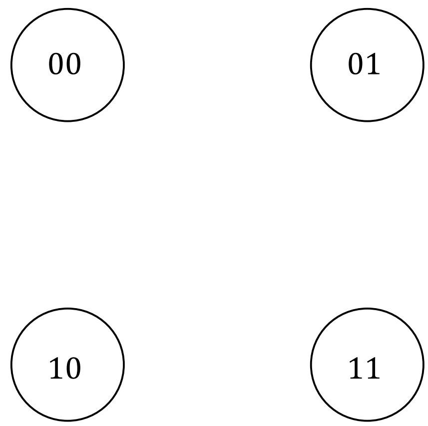
Problem 6

Consider the following sequential logic circuit. Let the input to the system be denoted as X. Use the codes Q_1Q_0 and $Q_1^*Q_0^*$ to represent the current and next states, respectively. Let the output of the system be denoted as Z. **Derive the state table and state diagram.** Complete the **timing trace** and **draw the timing diagram** *(on the next page)*.

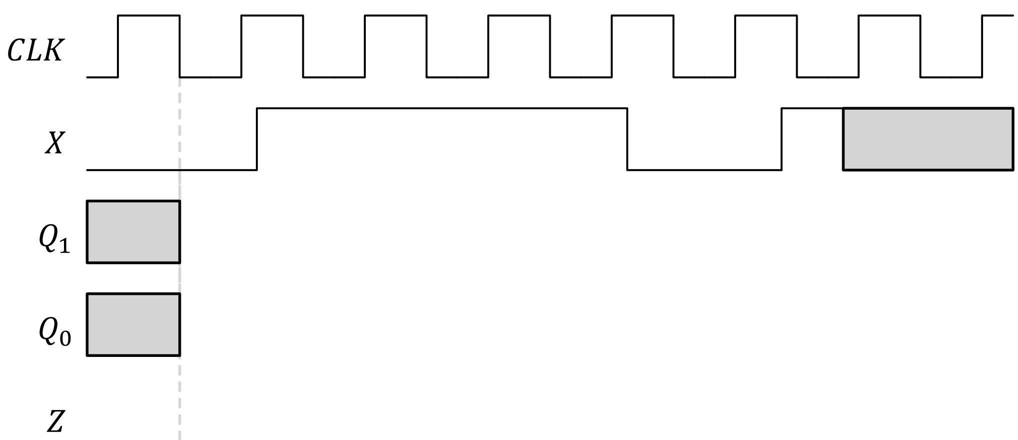


X	Q_1	Q_0	D_1	D_0	Z
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Current States (Q_1Q_0)	**Next States** $(Q_1^*Q_0^*)$		**Output** (Z)	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
0 0				
0 1				
1 0				
1 1				



X	0	1	1	1	1	1	1	1	0	?	?
Q_1	?										
Q_0	?										
Z											



Problem 7

Design a 3-bit counter that follows this sequence when input $X = 0$:

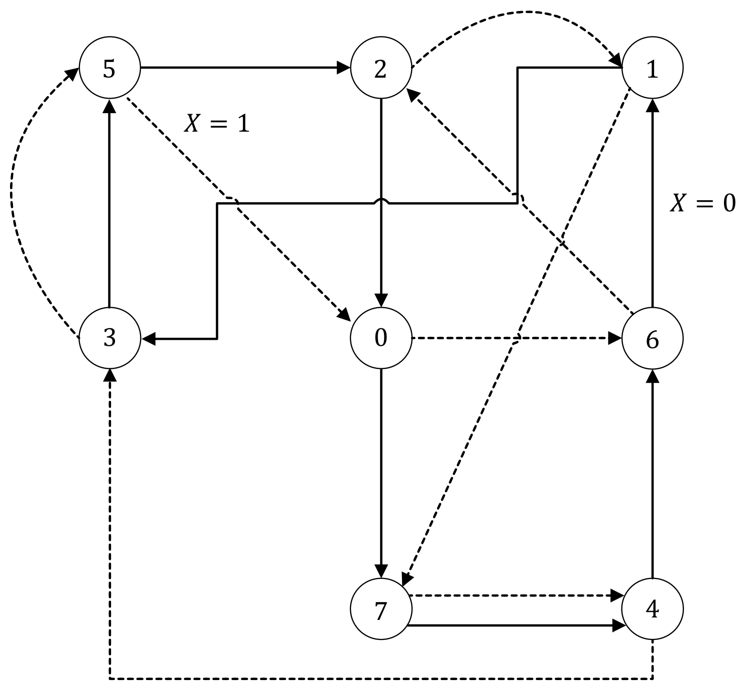
$$0 \to 2 \to 4 \to 6 \to 0 \text{ (repeats)}$$

When $X = 1$, it counts in reverse order. Use $Q_2Q_1Q_0$ to denote current states and $Q_2^*Q_1^*Q_0^*$ to denote next states. If the counter enters any unspecified state (1, 3, 5, 7), it should return to state 0 on the next clock cycle. **Draw the circuit.**

Area for drawing the circuit from Problem 7

Problem 8

Design a counter to produce the state transition shown below using D flip-flops. The sequence should follow the solid line when the input is 0, and follow the dashed line when the input is 1. Use $Q_2Q_1Q_0$ to denote the current states and $Q_2^*Q_1^*Q_0^*$ to denote the next states, and X to denote the input. **It is not necessary to draw the circuit.**



Problem 9

Design a 4-bit counter using D flip-flops that goes through the following sequence:

$$0000_2 \rightarrow 0011_2 \rightarrow 0110_2 \rightarrow 1100_2 \rightarrow 1111_2 \rightarrow 0000_2 \text{ (repeats)}$$

Use $Q_3Q_2Q_1Q_0$ to denote current states and $Q_3^*Q_2^*Q_1^*Q_0^*$ to denote next states. The state table must have 16 entries (consider unspecified states as don't cares). **Draw the circuit.** If the counter gets into one of the unspecified states by mistake, what will be the next state of the system?

Consider only two unspecified states in your state table: 0100_2 and 1000_2

Problem 10

Design a 3-bit counter using a mix of flip-flops:

- Use a J-K flip-flop for Q_2
- Use a D flip-flop for Q_1
- Use an S-R flip-flop for Q_0

The counter should follow this sequence when X = 1:

$$1 \to 3 \to 5 \to 7 \to 1 \text{ (repeats)}$$

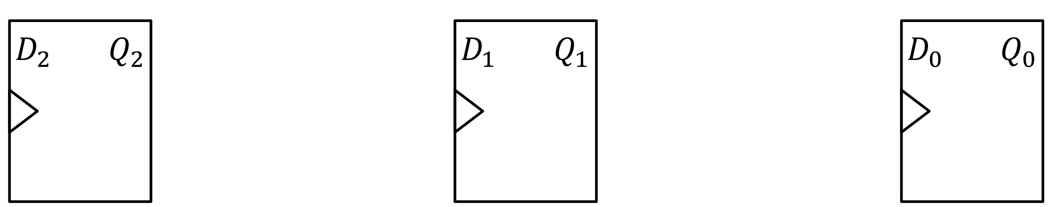
When X = 0, it should follow:

$$1 \to 7 \to 5 \to 3 \to 1 \text{ (repeats)}$$

If the counter gets into one of the unspecified states (i.e. 0,2,4,6) by mistake, what will be the next state of the system. **It is not necessary to draw the circuit.**

Problem 11

Design a 3-bit Gray code counter with an input denoted as X such that, when $X = 0$, the counter increments in the Gray code sequence, and when $X = 1$, it decrements in the Gray code sequence. Use $Q_2Q_1Q_0$ to denote the current states and $Q_2^*Q_1^*Q_0^*$ to denote the next states. **Draw the circuit.**



Problem 12

Design a sequential logic circuit for a vending machine that serves drinks priced at 15 baht. The machine:

- Accepts only 5, 10 baht coins
- Accumulates previously inserted money
- Issues item ($Z = 1$) when total reaches 15 baht or more
- After serving, returns to initial state (0 baht)

Use 2-bit codes Q_1Q_0 and $Q_1^*Q_0^*$ to indicate the current and next states respectively. Let the states represent:

State (Q_1Q_0)	Amount
00	0 baht
01	5 baht
10	10 baht
11	15 baht

1. Draw the state diagram
2. Design the circuit using J-K flip-flops
3. What happens when system starts in state 11?

This page is intentionally left blank for any purpose
(calculations, diagrams, notes, etc.) [1]

This page is intentionally left blank for any purpose
(calculations, diagrams, notes, etc.) [2]

Truth Tables for D, S-R, and J-K Latches/Flip Flops

Inputs	Outputs	
D	Q	$\bar{Q}$
0	0	1
1	1	0

Inputs		Outputs	
S	R	Q	$\bar{Q}$
0	0	Q_0	$\bar{Q}_0$
0	1	0	1
1	0	1	0
1	1	?	?

Inputs		Outputs	
J	K	Q	$\bar{Q}$
0	0	Q_0	$\bar{Q}_0$
0	1	0	1
1	0	1	0
1	1	$\bar{Q}_0$	Q_0

Transition Tables for D, S-R, and J-K Flip Flops

Desired State Transition		Excitation Variables				
Q	Q^*	D	S	R	J	K
0	0	0	0	X	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	1	1	X	0	X	0

List of Boolean Algebraic Laws

1. Commutative Laws
   a. $A + B = B + A$
   b. $AB = BA$

2. Associative Laws
   a. $A + (B + C) = (A + B) + C$
   b. $A(BC) = (AB)C$

3. Identity Laws
   a. $A + 0 = A$
   b. $A \cdot 1 = A$

4. Complementary Laws
   a. $A + \bar{A} = 1$
   b. $A\bar{A} = 0$

5. Idempotent Laws
   a. $A + A + \cdots + A = A$
   b. $AA \cdots A = A$

6. Involution Laws
   a. $\bar{\bar{A}} = A$

7. Null Laws
   a. $A + 1 = 1$
   b. $A \cdot 0 = 0$

8. Distributive Laws
   a. $A(B + C) = AB + AC$
   b. $(A + B)(A + C) = A + BC$
   c. $A + \bar{A}B = A + B$

9. Absorption Laws
   a. $A + AB = A$
   b. $A(A + B) = A$

10. De Morgan's Laws
    a. $\overline{A + B} = \bar{A}\bar{B}$
    b. $\overline{AB} = \bar{A} + \bar{B}$

11. Consensus Theorem
    a. $AB + \bar{A}C + BC = AB + \bar{A}C$

12. XOR / XNOR Gates
    a. $A \oplus B = \bar{A}B + A\bar{B}$
    b. $\overline{A \oplus B} = \bar{A}\bar{B} + AB$